AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor chip having a semiconductor element or an integrated circuit formed in the semiconductor chip, a low dielectric constant insulating film having a relative dielectric constant of about 3.5 or less formed directly on a surface of the semiconductor chip, a passivation film formed on a surface of the low dielectric constant insulating film to protect the low dielectric constant insulating film, and a plurality of first bump electrodes being provided on a surface of the passivation film;

a wiring board having a plurality of connecting electrodes being electrically connected to the bump electrodes, and a plurality of second bump electrodes formed on a side of the wiring board opposite to the connection electrodes, the plurality of second bump electrodes being electrically connected to the connecting electrodes; and

a resin molding filled in a space between the semiconductor chip and the wiring board, the electrically connected bump electrodes and the connecting electrodes being arranged in the space,

wherein the resin molding is formed of a resin having a flux function,-the resin is changing from liquid to solid when the bump electrodes are in a molten state, and a coefficient of elasticity of the resin is 20 MPa or more in a state where the resin is changing from liquid to solid when the bump electrodes are in the molten state.

2. (Canceled)

3. (Original) A semiconductor device according to claim 1, wherein an adhesion strength of the low dielectric constant insulating film to each of the semiconductor chip, the insulating film, and a metal film is 15 J/m^2 or less.

4-5. (Canceled)

6. (Original) A semiconductor device according to claim 1, wherein the resin molding comprises a first resin layer close to the semiconductor chip and a second resin layer close to the wiring board, and the second resin layer is a resin layer which does not contain a filler.

7. (Original) A semiconductor device according to claim 1, wherein the resin molding comprises a first resin layer close to the semiconductor chip, a second resin layer close to the wiring board, and a third resin layer interposed between the first resin layer and the second resin layer, and the third resin layer is a resin layer which does not contain a filler.

8. (Original) A semiconductor device according to claim 1, wherein the bump electrodes of the semiconductor chip are electrically connected to a plurality of connecting electrodes formed on the semiconductor chip, a part of the connecting electrodes are coated with a passivation film comprising at least one layer formed of an organic film.

9. (Withdrawn) A method of manufacturing a semiconductor device, comprising:

forming a plurality of bump electrodes on a surface of a semiconductor chip, in which a semiconductor element or an integrated circuit is formed, with a low dielectric constant insulating film formed on the surface of the semiconductor chip;

interposing a resin, which has a flux function between the semiconductor chip and a wiring board in which a plurality of connecting electrodes are formed;

aligning the bump electrodes and the respective connecting electrodes with the resin interposed therebetween, and pressing the semiconductor chip and the connecting electrodes against each other; and

heating the semiconductor chip and the wiring board to electrically connect the bump electrodes to the respective connecting electrodes, and to form a resin molding formed of the resin to fill a space between the semiconductor chip and the wiring board,

wherein the resin is a resin which changes from liquid to solid when the bump electrodes are in a molten state in connecting of the bump electrodes to the respective connecting electrodes.

10. (Withdrawn) A method of manufacturing a semiconductor device according to claim 9, wherein a relative dielectric constant of the low dielectric constant insulating film is about 3.5 or less.

11. (Withdrawn) A method of manufacturing a semiconductor device, according to claim 9, wherein a coefficient of elasticity of the resin is 20 MPa or more at normal temperature.

12. (Withdrawn) A method of manufacturing a semiconductor device, according to claim 9, wherein the heating the semiconductor chip and the wiring board is performed in a reflow furnace, and reflow conditions are a temperature of at least 200°C and a time of at least 60 seconds.

13. (Withdrawn) A method of manufacturing a semiconductor device, comprising:

forming a plurality of bump electrodes on a surface of a semiconductor chip, in which a semiconductor element or an integrated circuit is formed, with a low dielectric constant insulating film formed on the surface of the semiconductor chip;

interposing a first resin, which has a flux function, in the vicinity of the semiconductor chip, between the semiconductor chip and a wiring board in which a plurality of connecting electrodes are formed;

interposing a second resin, which has a flux functions and contains no filler, in the vicinity of the wiring board, between the semiconductor chip and the wiring boards in which the plurality of connecting electrodes are formed;

aligning the bump electrodes and the respective connecting electrodes with the fist and second resins interposed therebetween, and pressing the semiconductor chip and the connecting electrodes against each other; and

heating the semiconductor chip and the wiring board to electrically connect the bump electrodes to the respective connecting electrodes, and to form a resin molding formed of the first and second resins to fill a space between the semiconductor chip and the wiring board,

wherein the first and second resins are resins which change from liquid to solid when the bump electrodes are in a molten state in connecting of the bump electrodes to the respective connecting electrodes.

14. (Withdrawn) A method of manufacturing a semiconductor device according to claim 13, wherein a relative dielectric constant of the low dielectric constant insulating film is about 3.5 or less.

15. (Withdrawn) A method of manufacturing a semiconductor device, according to claim 13, wherein a coefficient of elasticity of the resin is 20 MPa or more at normal temperature.

16. (Withdrawn) A method of manufacturing a semiconductor device, according to claim 13, wherein the heating the semiconductor chip and the wiring board is performed in a reflow furnace, and reflow conditions are a temperature of at least 200°C and a time of at least 60 seconds.

17. (Withdrawn) A method of manufacturing a semiconductor device, comprising:

forming a plurality of bump electrodes on a surface of a semiconductor chip, in which a semiconductor element or an integrated circuit is formed, with a low dielectric constant insulating film formed on the surface of the semiconductor chip;

interposing a first resin, which has a flux function, in the vicinity of the wiring board, between the semiconductor chip and the wiring board in which the plurality of connecting electrodes are formed;

interposing a third resin, which has a flux function and contains no filler, between the first resin and the second resin;

aligning the bump electrodes and the respective connecting electrodes with the first, second and third resins interposed therebetween, and pressing the semiconductor chip and the connecting electrodes against each other; and

heating the semiconductor chip and the wiring board to electrically connect the bump electrodes to the respective connecting electrodes, and to form a resin molding formed of the first, second and third resins to fill a space between the semiconductor chip and the wiring board,

wherein the first, second and third resins are resins which change from liquid to solid when the bump electrodes are in a molten state in connecting of the bump electrodes to the respective connecting electrodes.

18. (Withdrawn) A method of manufacturing a semiconductor device according to claim 17, wherein a relative dielectric constant of the low dielectric constant insulating film is about 3.5 or less.

19. (Withdrawn) A method of manufacturing a semiconductor device, according to claim 17, wherein a coefficient of elasticity of the resin is 20 MPa or more at normal temperature.

20. (Withdrawn) A method of manufacturing a semiconductor device, according to claim 17, wherein the heating the semiconductor chip and the wiring board is performed in a reflow furnace, and reflow conditions are a temperature of at least 200°C and a time of at least 60 seconds.

21. (Currently Amended) A semiconductor device comprising:

a semiconductor chip in which a semiconductor element or an integrated circuit is formed;

a low K dielectric film formed on the semiconductor chip, the low K dielectric film having a wiring film formed therein;

a passivation film formed on the low K dielectric film, the passivation film having a pad formed therein;

a barrier film formed on the pad; and

a first bump electrode formed on the pad through the barrier film;

a wiring board having a at least one connecting electrode and at least one second bump electrode formed on a side of the wiring board opposite to the at least one connecting electrode, the at least one second bump electrode being electrically connected to the ~~bump~~ at least one connecting electrode; and

a resin molding filled in a space between the semiconductor chip and the wiring board, the electrically connected bump electrode and the connecting electrode being arranged in the space,

wherein the resin molding is formed of a resin having a flux function, the resin is changing from liquid to solid when the bump electrode is in a molten state, and a coefficient of elasticity of the resin is 20 MPa or more in a state where the resin is changing from liquid to solid when the bump electrode is in the molten state.

22. (Canceled)

23. (Currently Amended) A semiconductor device comprising:

a semiconductor chip in which a semiconductor element or an integrated circuit is formed;

a plurality of low K dielectric films formed on the semiconductor chip, the low K dielectric films having wiring films formed therein;

a plurality of passivation films formed on the low K dielectric films, each of the passivation films having a pad of a different material formed therein;

a barrier film formed in an uppermost passivation film of the plurality of passivation films;

a first bump electrode formed on the pad through the barrier film;

a wiring board having a at least one connecting electrode and at least one second bump electrode formed on a side of the wiring board opposite to the at least one connecting electrode, the at least one second bump electrode being electrically connected to the ~~bump~~ at least one connecting electrode; and

a resin molding filled in a space between the semiconductor chip and the wiring board, the electrically connected bump electrode and the connecting electrode being arranged in the space,

wherein the resin molding is formed of a resin having a flux function, the resin is changing from liquid to solid when the bump electrode is in a molten state, and a coefficient of elasticity of the resin is 20 MPa or more in a state where the resin is changing from liquid to solid when the bump electrode is in the molten state.

24. (Canceled)

25. (Previously Presented) A semiconductor device according to claim 21, wherein the barrier film is made of one selected from a group of Ti, Cr, Cu, Ni, Au, Pd, TiW, W, Ta, TaN, TiN or Nb, or a laminated film or alloy film thereof.

26. (Previously Presented) A semiconductor device according to claim 23, wherein the barrier film is made of one selected from a group of Ti, Cr, Cu, Ni, Au, Pd, TiW, W, Ta, TaN, TiN or Nb, or a laminated film or alloy film thereof.

27. (Previously Presented) A semiconductor device according to claim 1, wherein the low K dielectric film is made of one selected from a group of SiO_2, SiN, SiOC, HSQ (Hydrogen Silsesquioxane), Organic Silica, and porous HSQ, or a laminated film or porous film thereof.

28. (Previously Presented) A semiconductor device according to claim 21, wherein the low K dielectric film is made of one selected from a group of SiO_2, SiN, SiOC, HSQ (Hydrogen Silsesquioxane), Organic Silica, and porous HSQ, or a laminated film or porous film thereof.

29. (Previously Presented) A semiconductor device according to claim 23, wherein the low K dielectric film is made of one selected from a group of SiO_2, SiN, SiOC, HSQ (Hydrogen Silsesquioxane), Organic Silica, and porous HSQ, or a laminated film or porous film thereof.

30. (New) A semiconductor device according to claim 1, wherein the semiconductor chip further comprises a barrier metal layer comprising successive layers of a titanium film, a nickel film, and a palladium film, formed over a portion of the passivation film, and wherein the a plurality of bump electrodes are provided over the barrier metal layer.

31. (New) A semiconductor device according to claim 22, wherein the barrier film comprises successive layers of a titanium film, a nickel film, and a palladium film.

32. (New) A semiconductor device according to claim 23, wherein the barrier film comprises successive layers of a titanium film, a nickel film, and a palladium film.

33. (New) A semiconductor device according to claim 1, wherein the low k dielectric film is formed of a plurality of low k dielectric layers.

34. (New) A semiconductor device according to claim 21, wherein the low k dielectric film is formed of a plurality of low k dielectric layers.